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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,248	04/23/2004	Huilong Zhu	FIS920040081US1	3247

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EXAMINER	
SUCH, MATTHEW W	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,248	ZHU ET AL.	
	Examiner	Art Unit	
	Matthew W. Such	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *23 April 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

1. Applicant's election without traverse of Invention I in the reply filed on 12 January 2006 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8-12, 14, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hu (`802), who teaches a semiconductor circuit with a structure (Figs. 2A-2F and 4).

4. Regarding Claims 8, 12, 14 and 20, Hu (`802) teaches:

A first insulator bonded on a semiconductor substrate (Col. 3, Lines 26-30; Col. 8, Lines 31-35, 63-67);

A first semiconductor layer bonded on a first insulator (Col. 3, Lines 29-30; Col. 8, Lines 31-35, 63-67);

A second insulator bonded on a first insulator (Col. 5, Lines 1-4; Col. 8, Lines 39-40; Col. 9, Lines 4-5);

A second semiconductor layer bonded on a second insulator (Col. 5, Lines 1-4; Col. 8, Lines 41-42; Col. 9, Lines 6-7);

A second fin positioned in a second semiconductor layer (Element 42), wherein the height of the second fin correspond to the height of the second semiconductor layer (Col. 5, Lines 7-13);

A third fin stacked below a second fin in a first semiconductor layer (Element 40), wherein the height of the third fin corresponds to the height of the first semiconductor layer (Col. 2, Lines 44-46; Col. 5, Lines 7-13);

A plurality of stacked fin structures are formed on a substrate (Col. 2, Lines 11-14). The first fin corresponds to the second semiconductor layer of an adjacent stack structure;

5. Regarding Claim 9, Hu (`802) discloses devices showing stacked fins as forming a first finFET and a first fin in an adjacent device forms a second finFET.

6. Regarding Claim 10, Hu (`802) discloses devices showing a first finFET having a PMOS (p-channel finFET) and an adjacent second finFET having an NMOS (n-channel finFET).

7. Regarding Claim 19, Hu (`802) describes the semiconductor structure of claim 8, wherein:

A dopant is implanted into each of the fins to form a source region in a first exposed portion and a drain region in a second exposed portion, wherein a source and drain are separated by a channel region (Col. 4, Lines 4-29; Col. 8, Lines 36-38, 61-62; Col. 9, Lines 1-3, 26-27; Figs. 3 and 4);

A gate insulator is formed on either side of the fins (Col. 2, Lines 20-22; Col. 3, Lines 8-11, 56-61; Col. 4, Lines 1-3; Col. 8, Lines 39-40; Col. 9, Lines 17-18);

A gate conductor is formed on the gate insulator, thereby forming stack (Col. 2, Lines 20-22; Col. 3, Lines 12-15; 61-67; Col. 4, Lines 1-3; Col. 8, Lines 55-60; Col. 9, Lines 19-25).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (`802) in view of Fried (`259).

Hu (`802) teaches the device of claims 12 and 14 wherein the thickness of the layers, and hence transistor widths, can be adjusted independent of one another (Col. 3, Lines 30-35 and Col. 5, Lines 7-13). Hu is silent about teaching the specific semiconductor layer thickness ranges used for a particular custom device.

Fried (`259) teaches a CMOS finFET device where different fins have different thicknesses as shown in Figure 7b and that the typical fin dimension can be 50-200 nm thick (Col. 9, Lines 17-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to explicitly define a thickness range for a first semiconductor layer and a second semiconductor layer as disclosed by Hu ('802) to be at the lower end of the 50-200 nm range disclosed by Fried ('259). One skilled in the art would be motivated to do this in order to increase device density by miniaturizing the devices in all dimensions. Furthermore, it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu ('802) in view of Fried ('259).

Hu ('802) teaches the device of claim 8 wherein the crystallographic orientation of a fin may be selected in order to customize the carrier mobility of the device without defining explicit requirements for the relative mobilities of each layer in the stacked CMOS devices shown in Figure 4 (Col. 3, Lines 42-46).

Ko ('797) teaches a CMOS device having various crystallographic orientations to be different for the PFET and NFET (see entire publication). The stacks of semiconductor layers have unique crystallographic orientations, with the {110} layer (Paragraph 0024; Figs. 1-3, Element 110) below the {100} layer (Paragraph 0024; Figs. 1-3, Element 120). Ko further teaches that electron mobility is maximized in the {100} orientation and hole mobility is maximized in the {110} orientation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to explicitly define the crystallographic orientation of a first semiconductor layer (containing a first and second fin) and a second semiconductor layer

(containing a third fin) as disclosed by Hu ('806) to the {100} and {110} planes, respectively, as described by Ko ('797). Since the n-channel finFET device is oriented in the {100} the carrier mobility is maximized. The p-channel stacked finFET has an upper layer with a {100}, but also has a lower layer in the {110} maximizing the carrier mobility in that layer. Therefore, a CMOS device can be produced on a single substrate where both the p-channel and n-channel finFET devices have layers oriented to maximize carrier mobility to increase the device performance ('797 Col. 1, Paragraphs 0002-0004).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- '331 to Yeo also teaches the semiconductor circuit structure of as disclosed in claims 8-9, 11-12, 14, 19 and 20;
- '722 to Pham teaches a method for forming a finFET device structure;
- '789 to Gottsche teaches various configurations of finFET structures;
- '337 to Wang teaches methods for forming stacked fin structures having several semiconductor layers and insulator layers.
- '700 to Orlowski teaches a method for forming stacked finFET structures without including insulator layers to separate semiconductor layers.
- '351 and '259 to Fried teaches finFET structures utilizing different crystallographic orientations to optimize the carrier mobilities of the n-channel and p-channel devices.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is 571-272-8895. The examiner can normally be reached on Monday - Friday 8AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew W. Such
Examiner
Art Unit 2891

MWS
1/23/06

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